FIG. 1

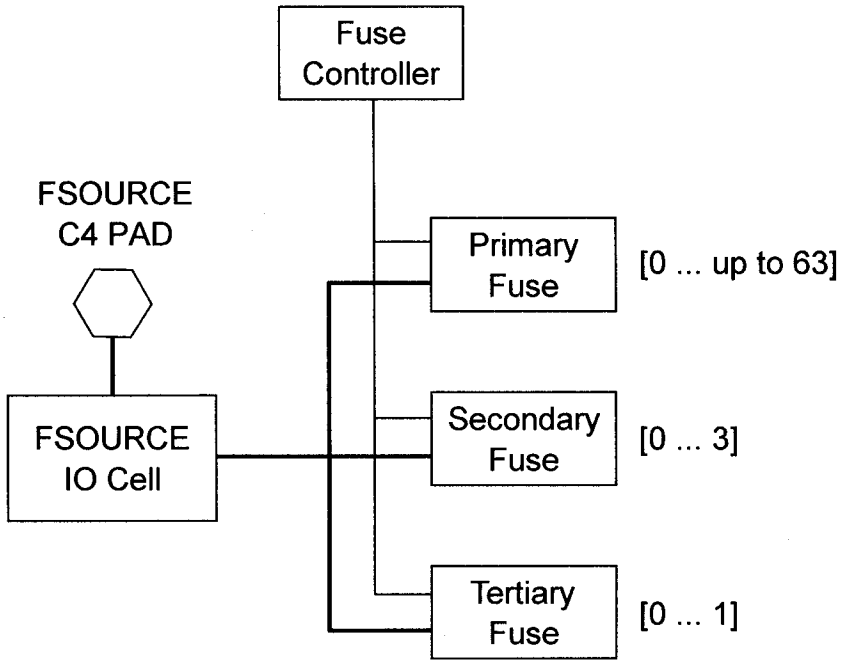
Fuse Controller
FSOURCE C4 PAD
Primary Fuse
[0 ... up to 63]
FSOURCE IO Cell
Secondary Fuse
[0 ... 3]
Tertiary Fuse
[0 ... 1]

FIG. 2

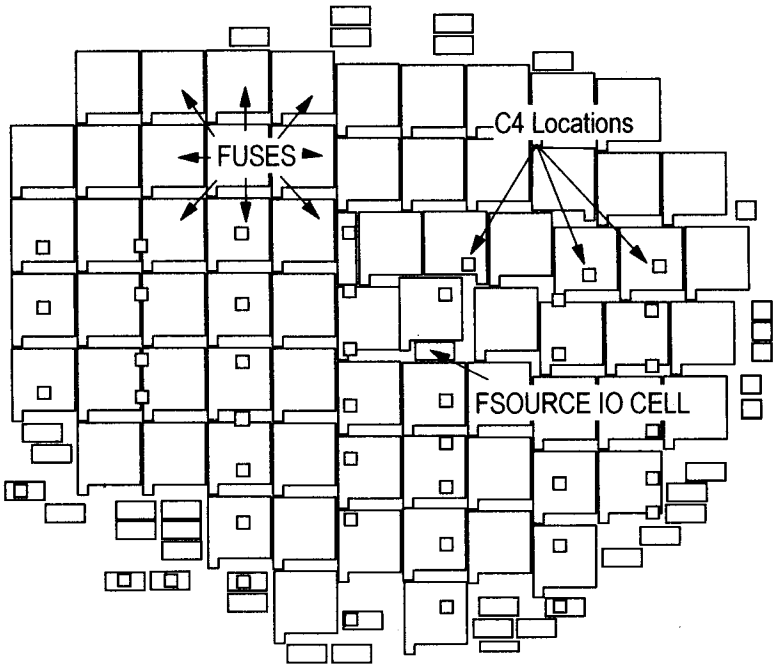

FIG. 3

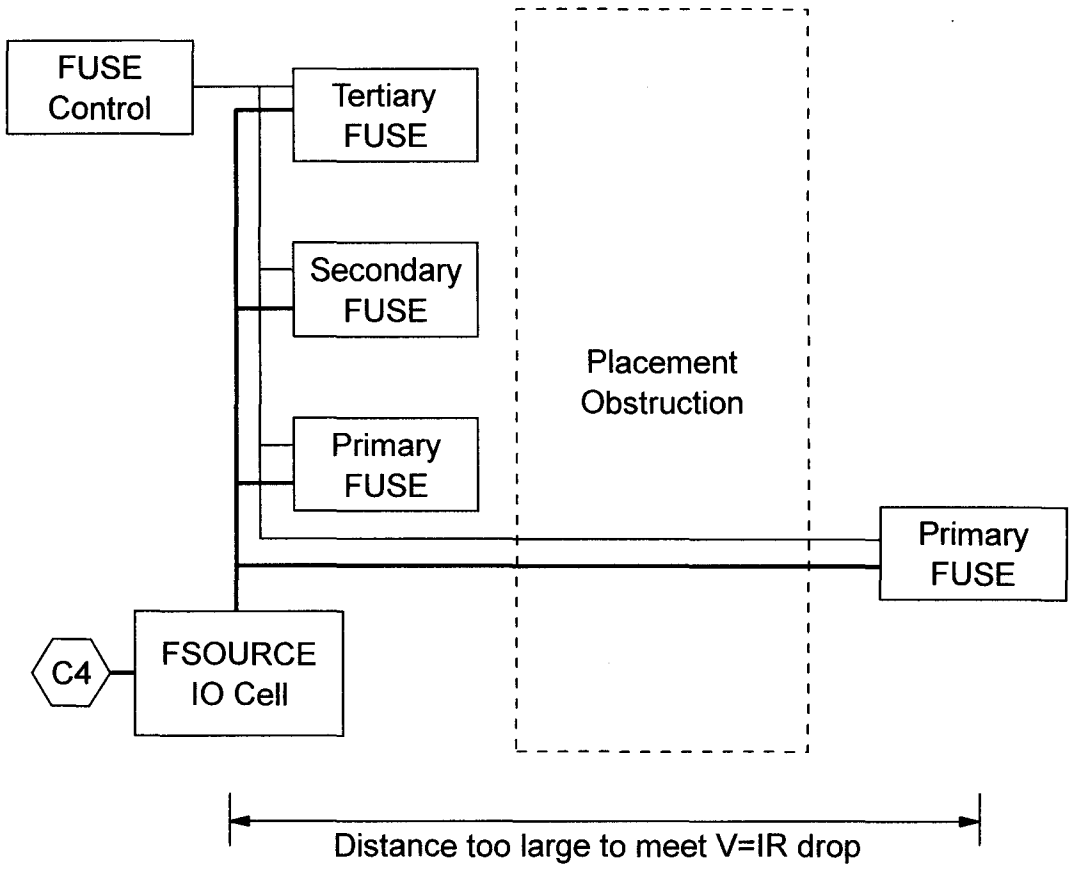
FUSE Control
Tertiary FUSE
Secondary FUSE
Primary FUSE
Placement Obstruction
Primary FUSE
C4
FSOURCE IO Cell
Distance too large to meet V=IR drop

FIG. 4

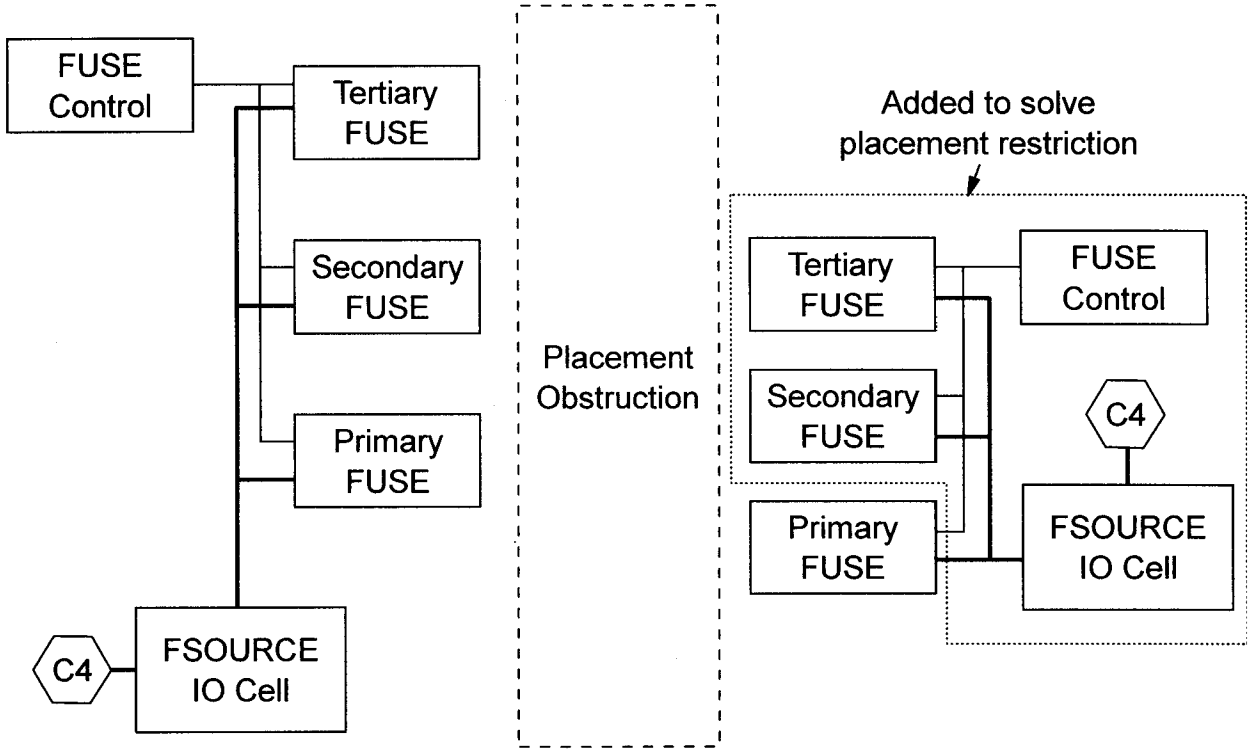
FUSE Control
Tertiary FUSE
Secondary FUSE
Primary FUSE
C4
FSOURCE IO Cell
Placement Obstruction
Added to solve placement restriction
Tertiary FUSE
FUSE Control
Secondary FUSE
C4
Primary FUSE
FSOURCE IO Cell

FIG. 5

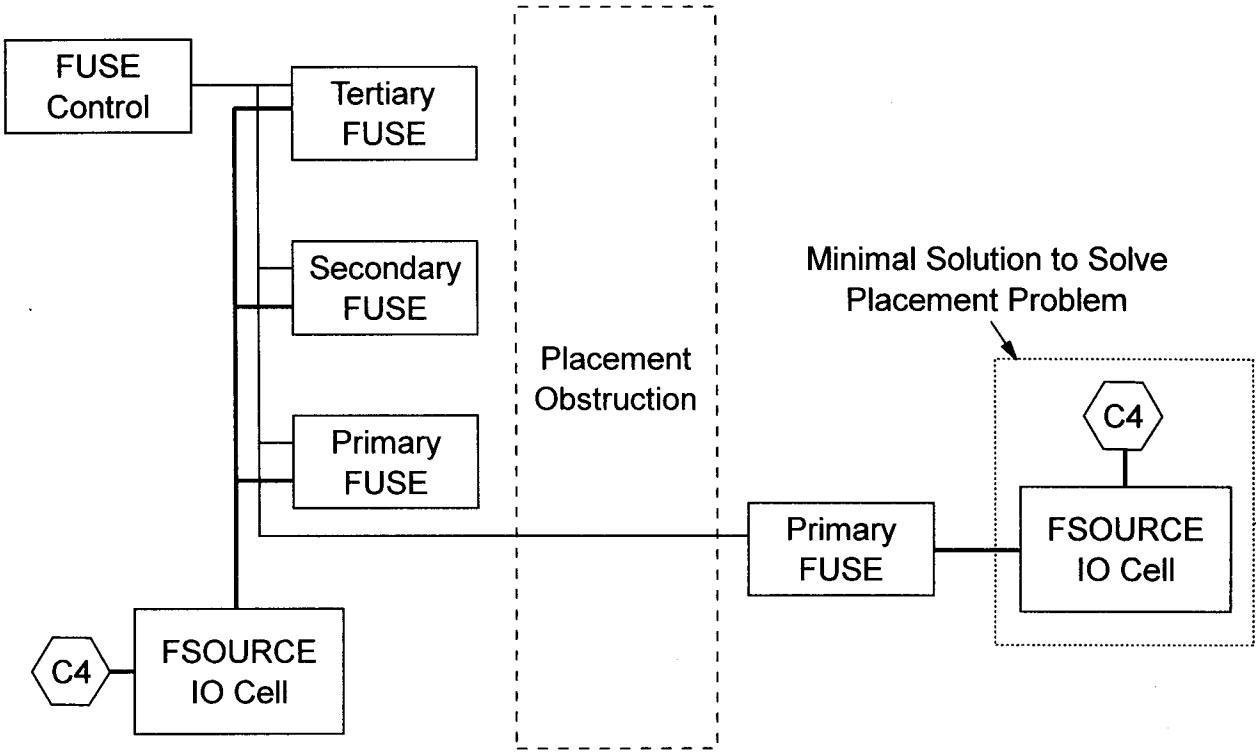
FUSE Control
Tertiary FUSE
Secondary FUSE
Primary FUSE
C4
FSOURCE IO Cell
Placement Obstruction
Minimal Solution to Solve Placement Problem
C4
FSOURCE IO Cell
Primary FUSE

FIG. 6

1. Determine P and N.

P = number of primary fuse macros
N = maximum allowable number of primary fuse macros per FSOURCE connection

2. Compare P and N and create FSOURCE C4s.

If P<N, create one FSOURCE C4
If P>N, create P/N (rounded up to nearest whole number) FSOURCE C4s

3. Divide primary fuse macros among FSOURCE C4s.

4. Floorplan the chip.

If normal floorplanning constraints cannot be met, go on to step 5.

5. Create on new FSOURCE C4.

6. Divide primary fuse macros among FSOURCE C4s.

7. Repeat steps 4-6 until normal floorplanning constraints are met in Step 5.